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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,615	06/09/2000	Laurent Six	TI-29030	2796

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EXAMINER	
BATAILLE, PIERRE MICHE	
ART UNIT	**PAPER NUMBER**
2186	14

DATE MAILED: 07/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/591,615	SIX ET AL.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *7* is/are withdrawn from consideration.

5)☒ Claim(s) *5* is/are allowed.

6)☒ Claim(s) *1-4,6 and 8-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is taken in response to Applicant amendment filed on May 25, 2004. Claims 1-6 and 8-12 are pending in the application under prosecution as claim 7 has been canceled.

Response to Arguments

2. Applicant's arguments filed with respect to claims 1-4, 6, and 8-12 have been fully considered but they are not deemed to be persuasive for at least the following.

Claim 5, having been rewritten in independent form, is allowable.

Applicant argues that Moyer (US 5,375,216) fails to teach the claimed features required in claims 1 and 8, as the Office Action fails to indicated where Moyer discloses a plurality of requestor circuits. In contrast, the Office Action is clear, indicating a plurality of requestor circuits taught in Moyer as "processor circuit and plurality of peripheral circuits". Peripheral circuit is any circuit (user program, controller, bus device, memory device, ...) operable to initiate request operations [Col. 1, Lines 24-38; Col. 5, Lines 9-12]. Moyer clearly teaches control operation of a memory controller or a similar processing system.

Yet the reference emphasizes on the data processor (a singular) operating in supervisor mode and normal mode, but applicant ignores that Moyer discloses: limiting exclusive access to only a small portion of memory, in one mode of operation, where

only data processor has access and where no external processor may access the data therein (Col. 11, Line 44-46).

Moyer teaches each cache control instruction encoded as a load operation having a predetermined size access to a predetermined register with the size signal to implement an external smart memory controller to provide control and data information for future cache transactions (col. 4, Lines 6-63; Col. 18, Lines 62-67).

Moyer teaches access of data cache unit is restricted to only a small portion of memory referred to as "user memory" such that the second portion is not selected in response to the access mode circuit where said second portion is not being addressed and the location pertaining to the second portion is not activated in user mode [Col. 10, Lines 42-51].

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 6, 8-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Moyer et al (US 5,375,216).

With respect to claim 8, Moyer teaches a digital system having a memory circuit that is shared by a plurality of requestor circuits (processor circuit and plurality of peripheral circuits), comprising the steps of: sharing access to the memory circuit between the

plurality of requestor circuits when the digital system is in a first mode of operation [(in the supervisor mode of operation, access to data cache unit 24 and register file 32 is unrestricted) [Col. 10, Lines 49-51]; selecting a first portion of the memory circuit responsive to a size parameter stored in a register, such that a second portion of the memory circuit in not selected [(each control instruction having a predetermined size access to a predetermined register) [Col. 10, Lines 55-59; Col. 4, Line 61-63]; and limiting access to a first portion of the memory circuit to only a first requester of the plurality of requestors when the digital system is in a second mode of operation [(in user mode, access of data cache unit 24 is restricted to only a small portion of memory referred to as "user memory" and a limited number of registers in register file 32) [Col. 10, Lines 42-45].

With respect to claim 1, Moyer teaches a system and method operating a digital system having a memory circuit comprising a plurality of requestors (processor circuit and plurality of peripheral circuits); a scheduling circuit (sequencer 34) operable to sequentially schedule memory access to the memory circuit [Col. 9, Lines 30-48]; a selection circuit and access mode circuitry for: indicating shared access to the memory circuit between the plurality of requestors circuits when the digital system in a first mode of operation and for selecting a portion of the memory responsive to a size parameter stored in a register (*register file 32*) [(each control instruction having a predetermined size access to a predetermined register) [Col. 10, Lines 55-59; Col. 4, Line 61-63] such that the second portion is not selected; and limiting access to the first portion of the memory circuit to only a first requestor in a second mode of operation [(in the supervisor mode of operation, access to data cache unit 24 and register file 32 is unrestricted) Col. 10, Lines 49-51; (in user mode,

access of data cache unit 24 is restricted to only a small portion of memory referred to as "user memory" and a limited number of registers in register file 32) [Col. 10, Lines 42-45].

With respect to claims 2-4, 6 and 9-12, Moyer teaches, in user mode, access of data cache unit 24 is restricted to only a small portion of memory referred to as "user memory" and a limited number of registers in register file 32 such that the second portion is not selected in response to the access mode circuit [Col. 10, Lines 42-45] said second portion would inherently placed in low power mode as it is not being addressed and the location pertaining to the second portion is not activated; and in the supervisor mode of operation, access to data cache unit 24 and register file 32 is unrestricted, i.e. the entire memory circuit is operable for sequential access [Col. 10, Lines 49-51].

Allowable Subject Matter

5. Claim 5 is allowable.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,202,130 (Scales, III et al) teaching data processing system for processing vector data and method therefor

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 305-0134. The examiner can normally be reached on Tue-Fri (7:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

July 10, 2004

PIERRE BATAILLE
PRIMARY EXAMINER